LP3853, LP3856

LP3853/LP3856 3A Fast Response Ultra Low Dropout Linear Regulators

Literature Number: SNVS173F
General Description

The LP3853/LP3856 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3853/LP3856 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3853/LP3856 to operate under extremely low dropout conditions.

**Dropout Voltage:** Ultra low dropout voltage; typically 39mV at 300mA load current and 390mV at 3A load current.

**Ground Pin Current:** Typically 4mA at 3A load current.

**Shutdown Mode:** Typically 10nA quiescent current when the shutdown pin is pulled low.

**Error Flag:** Error flag goes low when the output voltage drops 10% below nominal value.

**Sense:** Sense pin improves regulation at remote loads.

**Precision Output Voltage:** Multiple output voltage options are available ranging from 1.8V to 5.0V with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

Features

- Ultra low dropout voltage
- Stable with selected ceramic capacitors
- Low ground pin current
- Load regulation of 0.08%
- 10nA quiescent current in shutdown mode
- Guaranteed output current of 3A DC
- Available in TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- Error flag indicates output status
- Sense option improves load regulation
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Microprocessor power supplies
- Stable with ceramic output capacitors
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits

```
3.3V ± 10%

C_IN = 10 μF

V_IN

SD

V_OUT

ERROR

C_OUT = 10 μF

V_OUT = 1.8V, 3.0A

* TANTALUM OR CERAMIC

** SD and ERROR pins must be pulled high through a 10kΩ pull-up resistor. Connect the ERROR pin to ground if this function is not used. See Application Hints for more information.
```
**SD** pin must be pulled high through a 10kΩ pull-up resistor. See Application Hints for more information.

**Connection Diagrams**

**Pin Description for TO220-5 and TO263-5 Packages**

<table>
<thead>
<tr>
<th>Pin #</th>
<th>LP3853</th>
<th>LP3856</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Function</td>
</tr>
<tr>
<td>1</td>
<td>SD</td>
<td>Shutdown</td>
</tr>
<tr>
<td>2</td>
<td>$V_{IN}$</td>
<td>Input Supply</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>$V_{OUT}$</td>
<td>Output Voltage</td>
</tr>
<tr>
<td>5</td>
<td>ERROR</td>
<td>ERROR Flag</td>
</tr>
</tbody>
</table>
Ordering Information

TABLE 1. Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>Order Number</th>
<th>Description (Current, Option)</th>
<th>Package Type</th>
<th>Package Marking</th>
<th>Supplied As</th>
</tr>
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<tbody>
<tr>
<td>5.0</td>
<td>LP3853ES-5.0</td>
<td>3A, Error Flag</td>
<td>TO263-5</td>
<td>LP3853ES-5.0</td>
<td>Rail</td>
</tr>
<tr>
<td>5.0</td>
<td>LP3853ESX-5.0</td>
<td>3A, Error Flag</td>
<td>TO263-5</td>
<td>LP3853ES-5.0</td>
<td>Tape and Reel</td>
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<tr>
<td>3.3</td>
<td>LP3853ES-3.3</td>
<td>3A, Error Flag</td>
<td>TO263-5</td>
<td>LP3853ES-3.3</td>
<td>Rail</td>
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<td>2.5</td>
<td>LP3853ES-2.5</td>
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<td>LP3853ES-2.5</td>
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<td>TO263-5</td>
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<td>Tape and Reel</td>
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<tr>
<td>1.8</td>
<td>LP3853ES-1.8</td>
<td>3A, Error Flag</td>
<td>TO263-5</td>
<td>LP3853ES-1.8</td>
<td>Rail</td>
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<td>Rail</td>
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<td>3A, SENSE</td>
<td>TO263-5</td>
<td>LP3856ESX-1.8</td>
<td>Tape and Reel</td>
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<tr>
<td>5.0</td>
<td>LP3853ET-5.0</td>
<td>3A, Error Flag</td>
<td>TO220-5</td>
<td>LP3853ET-5.0</td>
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<td>TO220-5</td>
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<td>Rail</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Storage Temperature Range: −65°C to +150°C
- Lead Temperature: (Soldering, 5 sec.) 260°C
- ESD Rating (Note 3): 2 kV
- Power Dissipation (Note 2): Internally Limited
- Input Supply Voltage (Survival): −0.3V to +7.5V
- Shutdown Input Voltage (Survival): −0.3V to 7.5V
- Output Voltage (Survival), (Note 6), (Note 7): V<sub>IN</sub>, V<sub>OUT</sub>
- Maximum Voltage for ERROR Pin: V<sub>IN</sub>
- Maximum Voltage for SENSE Pin: V<sub>OUT</sub>

### Electrical Characteristics

#### LP3853/LP3856

Limits in standard typeface are for T<sub>J</sub> = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V<sub>IN</sub> = V<sub>O(NOM)</sub> + 1V, I<sub>L</sub> = 10 mA, C<sub>OUT</sub> = 10µF, V<sub>SD</sub> = 2V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter (Note 8)</th>
<th>Conditions</th>
<th>Typ (Note 4)</th>
<th>LP3853/6 (Note 5)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Voltage Tolerance</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ 7.0V</td>
<td>0</td>
<td>-1.5</td>
<td>+1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 mA ≤ I&lt;sub&gt;L&lt;/sub&gt; ≤ 3A</td>
<td></td>
<td>-3.0</td>
<td>+3.0</td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Output Voltage Line Regulation</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ 7.0V</td>
<td>0.02</td>
<td>0.06</td>
<td>%</td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt;/ΔI&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output Voltage Load Regulation</td>
<td>10 mA ≤ I&lt;sub&gt;L&lt;/sub&gt; ≤ 3A</td>
<td>0.08</td>
<td>0.14</td>
<td>%</td>
</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt; - V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Dropout Voltage</td>
<td>I&lt;sub&gt;L&lt;/sub&gt; = 300 mA</td>
<td>39</td>
<td>50</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;L&lt;/sub&gt; = 3A</td>
<td>390</td>
<td>450</td>
<td>600</td>
</tr>
<tr>
<td>I&lt;sub&gt;GND&lt;/sub&gt;</td>
<td>Ground Pin Current In Normal Operation Mode</td>
<td>I&lt;sub&gt;L&lt;/sub&gt; = 300 mA</td>
<td>4</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;L&lt;/sub&gt; = 3A</td>
<td>4</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>I&lt;sub&gt;GND&lt;/sub&gt;</td>
<td>Ground Pin Current In Shutdown Mode</td>
<td>V&lt;sub&gt;SD&lt;/sub&gt; ≤ 0.3V</td>
<td>0.01</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>−40°C ≤ T&lt;sub&gt;J&lt;/sub&gt; ≤ 85°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;PK&lt;/sub&gt;</td>
<td>Peak Output Current</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; ≥ V&lt;sub&gt;O(NOM)&lt;/sub&gt; - 4%</td>
<td>4.5</td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

### Short Circuit Protection

- I<sub>SC</sub> | Short Circuit Current | 6 | A |
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 4)</th>
<th>LP3853/6 (Note 5)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
</tbody>
</table>

**Shutdown Input**

- **V<sub>SDT</sub>** Shutdown Threshold
  - V<sub>SDT</sub> Rising from 0.3V until Output = ON
  - Min: 1.3
  - Max: 2
  - Units: V
  - **Note 4**: Typical numbers are at 25°C and represent the most likely parametric norm.

- **T<sub>dOFF</sub>** Turn-off delay
  - I<sub>L</sub> = 3A
  - Min: 20
  - Units: µs

- **T<sub>dON</sub>** Turn-on delay
  - I<sub>L</sub> = 3A
  - Min: 25
  - Units: µs

- **I<sub>SD</sub>** SD Input Current
  - V<sub>SD</sub> = V<sub>IN</sub>
  - Min: 1
  - Units: nA

**Error Flag**

- **V<sub>T</sub>** Threshold
  - Min: 10
  - Max: 16
  - Units: %
  - **Note 9**: Error Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.

- **V<sub>TH</sub>** Threshold Hysteresis
  - Min: 5
  - Max: 2
  - Units: %

- **V<sub>EF(Sat)</sub>** Error Flag Saturation
  - I<sub>sink</sub> = 100µA
  - Min: 0.02
  - Max: 0.1
  - Units: V

- **T<sub>d</sub>** Flag Reset Delay
  - Min: 1
  - Units: µs

- **I<sub>max</sub>** Error Flag Pin Sink Current
  - V<sub>Error</sub> = 0.5V
  - Min: 1
  - Units: mA

**AC Parameters**

- **PSRR** Ripple Rejection
  - V<sub>IN</sub> = V<sub>OUT</sub> + 1V
  - C<sub>OUT</sub> = 10uF
  - V<sub>OUT</sub> = 3.3V, f = 120Hz
  - Min: 73
  - Units: dB

- **P<sub>noff</sub>** Output Noise Density
  - f = 120Hz
  - Min: 0.8
  - Units: µV

- **e<sub>n</sub>** Output Noise Voltage
  - BW = 10Hz – 100kHz
  - V<sub>OUT</sub> = 2.5V
  - Min: 150
  - Units: µV (rms)

  - BW = 300Hz – 300kHz
  - V<sub>OUT</sub> = 2.5V
  - Min: 100

**Notes**:

- **Note 1**: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

- **Note 2**: At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ<sub>jA</sub> = 50°C/W (with 0.5in<sup>2</sup>, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at θ<sub>jA</sub> = 60°C/W (with 0.5in<sup>2</sup>, 1oz. copper area), junction-to-ambient. See Application Hints.

- **Note 3**: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

- **Note 4**: Typical numbers are at 25°C and represent the most likely parametric norm.

- **Note 5**: Limits are guaranteed by testing, design, or statistical correlation.

- **Note 6**: If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.

- **Note 7**: The output PMOS structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

- **Note 8**: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

- **Note 9**: Error Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.

- **Note 10**: Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

- **Note 11**: The minimum operating value for V<sub>IN</sub> is equal to either [V<sub>OUT(MIN)</sub> + V<sub>DROPOUT</sub>] or 2.5V, whichever is greater.
Typical Performance Characteristics

Unless otherwise specified: \( T_J = 25^\circ C, \) \( C_{OUT} = 10\mu F, \)
\( C_{IN} = 10\mu F, \) S/D pin is tied to \( V_{IN}, \) \( V_{OUT} = 2.5V, \) \( V_{IN} = V_{O(NOM)} + 1V, \) \( I_L = 10\ mA. \)
DC Line Regulation vs Temperature

Noise vs Frequency

Load Transient Response
$C_{IN} = C_{OUT} = 10\mu F$, OSCON

Load Transient Response
$C_{IN} = C_{OUT} = 100\mu F$, POSCAP

$V_{IN}$ vs $V_{OUT}$ Over Temperature

$C_{IN} = C_{OUT} = 10\mu F$, OSCON

$C_{IN} = C_{OUT} = 100\mu F$, POSCAP
Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 10µF is required. Ceramic or Tantalum may be used, and capacitance may be increased without limit.

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum amount of output capacitance that can be used for stable operation is 10µF. For general usage across all load currents and operating conditions, the part was characterized using a 10µF Tantalum input capacitor. The minimum and maximum stable ESR range for the output capacitor was then measured which kept the device stable, assuming any output capacitor whose value is greater than 10µF (see Figure 1 below).

If the maximum load current is 2A and a 10µF ceramic input capacitor is used, the regulator will be stable with ceramic output capacitor values from 10µF up to about 50µF. At 3A of load current, the ratio of input to output capacitance required approaches 1:1, meaning that whatever amount of ceramic output capacitance is used must also be provided at the input for stable operation. For load currents between 1A, 2A, and 3A, interpolation may be used to approximate values on the graph. When calculating the total ceramic output capacitance present in an application, it is necessary to include any ceramic bypass capacitors connected to the regulator output.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see Capacitor Characteristics section).

CAPACITOR CHARACTERISTICS

CERAMIC: For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated...
It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem.

Since high current flows through the traces going into $V_{IN}$ and coming from $V_{OUT}$, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

**RFI/EMI SUSCEPTIBILITY**

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

**OUTPUT NOISE**

Noise is specified in two ways-

- **Spot Noise** or Output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- **Total output Noise** or Broad-band noise is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units $\mu$V/Hz or nV/Hz and total output noise is measured in $\mu$V(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal...
Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3853/LP3856 achieves low noise performance and low quiescent current operation. The total output noise specification for LP3853/LP3856 is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

**SHORT-CIRCUIT PROTECTION**

The LP3853 and LP3856 are short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

**ERROR FLAG OPERATION**

The LP3853/LP3856 produces a logic low signal at the Error Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in Figure 3 shows the relationship between the ERROR flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal Error flag comparator has an open drain output stage. Hence, the ERROR pin should be pulled high through a pull up resistor. Although the ERROR flag pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of 10kΩ to 1MΩ. **The ERROR pin must be connected to ground if this function is not used.** It should also be noted that when the shutdown pin is pulled low, the ERROR pin is forced to be invalid for reasons of saving power in shutdown mode.

**SENSE PIN**

In applications where the regulator output is not very close to the load, LP3856 can provide better remote load regulation using the SENSE pin. Figure 4 depicts the advantage of the SENSE option. LP3853 regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is 100mΩ, the voltage at the remote load will be 3V with 3A of load current, I_{LOAD}. The LP3856 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 4. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin.
FIGURE 4. Improving remote load regulation using LP3856

SHUTDOWN OPERATION
A CMOS Logic low level signal at the Shutdown (SD) pin will turn-off the regulator. Pin SD must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used. The Shutdown (SD) pin threshold has no voltage hysteresis. If the Shutdown pin is actively driven, the voltage transition must rise and fall cleanly and promptly.

DROPOUT VOLTAGE
The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

REVERSE CURRENT PATH
The internal MOSFET in LP3853 and LP3856 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

POWER DISSIPATION/HEATSINKING
LP3853 and LP3856 can deliver a continuous current of 3A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_IN - V_OUT)I_{OUT} + (V_IN)I_{GND}$$

where $I_{GND}$ is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise ($T_{Rmax}$) depends on the maximum ambient temperature ($T_{Amax}$) of the application, and the maximum allowable junction temperature ($T_{Jmax}$):

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction to ambient Thermal Resistance, $\theta_{JA}$, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D$$

LP3853 and LP3856 are available in TO-220 and TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of $\theta_{JA}$ calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable $\theta_{JA}$ falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE
The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{JA}$ will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance:

$$\theta_{JA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}$$

In this equation, $\theta_{CH}$ is the thermal resistance from the case to the surface of the heat sink and $\theta_{JC}$ is the thermal resistance from the junction to the surface of the case. $\theta_{JC}$ is about 3°C/W for a TO220 package. The value for $\theta_{CH}$ depends on method of attachment, insulator, etc. $\theta_{CH}$ varies between 1.5°C/W and 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING TO-263 PACKAGE
The TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 5 shows a curve for the $\theta_{JA}$ of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.
As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for $\theta_{JA}$ for the TO-263 package mounted to a PCB is 32°C/W.

Figure 6 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming $\theta_{JA}$ is 35°C/W and the maximum junction temperature is 125°C.
Physical Dimensions inches (millimeters) unless otherwise noted

TO220 5-lead, Molded, Stagger Bend Package (TO220-5)
NS Package Number T05D

For Order Numbers, refer to the “Ordering Information” section of this document.
TO263 5-Lead, Molded, Surface Mount Package (TO263-5)

For Order Numbers, refer to the “Ordering Information” section of this document.
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